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Title : FREQUENCY SHIFTING CIRCUIT AND METHOD  
Assignee : NEC Corporation

Enclosed herewith please find the following documents in the above-identified application for United States Letters Patent:

- 27 Pages of Specification including Abstract and Claims
- 14 Numbered Claims Calculated as 14 Claims for Fee Purposes
- 8 Sheets of Drawing Containing Figures 1 to 10.
- X Declaration and Power of Attorney
- X Priority is Claimed under 35 U.S.C. §119:
- Convention Date April 15, 1999 for Japan Appln. S.N. 11-108333
- Certified Priority Application
- Verified Statement Claiming Small Entity Status under 37 C.F.R. §1.27.
- X Assignment
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## FREQUENCY SHIFTING CIRCUIT AND METHOD

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to frequency shifting techniques suitable for a demodulator of a receiver in a multi-carrier communications system.

#### 2. Description of the Related Art

In next generation mobile communications systems, much attention is focused on IMT-2000 (International Mobile Telecommunications-2000) system defined by ITU-R TG 8/1. There have been proposed several systems such as W-CDMA (Wideband-Code Division Multiple Access) and cdma2000, which may employ a multi-carrier scheme to allow high-speed data transmission.

The cdma2000 system is designed to realize upward compatibility with cdmaOne conforming to IS-95 and is likely to employ a multi-carrier scheme in downlink transmission. An example of the multi-carrier scheme in CDMA communications is shown in Fig. 10. In this example, it is assumed that the frequency offset of sub-carriers (Carrier-1 and Carrier+1) from the center carrier is 1.25 MHz and the chip rate is 1.2288 Mcps. In the cdmaOne communications, data can be transmitted at 14.4 kbps using a single carrier (center carrier). In contrast, the multi-carrier cdma system allows a maximum data rate of 43.2 kbps using three carriers.

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To successfully receive such a multi-carrier signal, the simplest is to provide a different receiver dedicated to each of a plurality of carriers. However, the number of receivers to be needed increases as the number of carriers increases, resulting in increased amount of hardware and increased power consumption.

Another solution is that a single receiver is provided to receive signals on all the carriers and a digital baseband processor individually processes the received signals according to carrier frequencies. There have been proposed several methods for handling a received signal for each of a plurality of carriers.

In Japanese Patent Unexamined Publication No. 7-221806, a demodulator employing time division multiplexing scheme has been disclosed. More specifically, the respective carriers are identified by time slots of the time division multiplexing scheme and I- and Q-component signals for each carrier are frequency-shifted to produce baseband I- and Q-component signals for the center carrier by phase rotation computation.

In Japanese Patent Unexamined Publication No. 8-46654, a demodulator employing a carrier selection means at an input stage has been disclosed. More specifically, one of a plurality of carriers is selected according to carrier designation data. Only a signal of the selected carrier is subjected to quadrature frequency conversion to produce I- and Q-component signals and the I- and Q-component signals for each carrier are frequency-shifted to produce baseband I- and Q-component signals

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5 receiver has been disclosed. The FFT can be used to separate  
a plurality of carriers.

10 the circuit, increase of the circuit scale, and increase of power  
consumption. A multi carrier receiver having a small circuit  
scale and saving power is not realized.

## SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide  
15 a frequency shifting circuit and method suitable for a digital  
demodulator in a multi-carrier communications system.

Another object of the present invention is to provide a frequency shifting circuit and method suitable for a small-sized portable CDMA receiver.

20           According to an aspect of the present invention, a digital circuit for shifting a frequency band of a signal vector to a predetermined frequency band, wherein the signal vector is determined by a pair of I (in-phase) and Q (quadrature) components on I-Q plane, includes:

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a control data generator for generating control data from a frequency difference between the frequency band and the predetermined frequency band; and

5 a signal vector rotator for rotating the signal vector on the I-Q plane by an angle determined depending on the control data to produce an output signal vector in the predetermined frequency band.

According to another aspect of the present invention a digital circuit for shifting a plurality of frequency bands of input signal vectors to a predetermined center frequency band to produce an output signal vector for each frequency band, wherein each of the input signal vectors is determined by a pair of I (in-phase) and Q (quadrature) components on I-Q plane, includes:

15 an analog-to-digital converter for converting analog signal vectors to the input signal vectors according to a predetermined sampling clock;

a control data generator for generating control data from a frequency difference between each of the plurality of frequency bands and the predetermined center frequency band;

20 a signal vector rotator corresponding to each of the plurality of frequency bands, for rotating the input signal vectors on the I-Q plane by an angle determined depending on corresponding control data to shift the frequency bands of the input signal vectors to the predetermined center frequency band; and

a band-pass filter corresponding to the signal vector, for

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receiving an output of the signal vector rotator and passing an output signal vector of the predetermined center frequency band.

The control data generator preferably includes a phase data generator for generating phase data  $\Phi$  from the frequency difference in synchronization with the predetermined sampling clock, and a converter for converting the phase data  $\Phi$  to the control data  $D$  consisting of a plurality of control bits  $D_k$ , where  $-1 \leq k \leq m-2$  ( $m$  is a positive integer).

The phase data generator preferably generates the phase data  $\Phi$  by computing an integral multiple of a unit angle  $\Delta$  which is obtained from a frequency shift  $\delta$  per period of the predetermined sampling clock, wherein the unit angle  $\Delta$  is represented by  $360^\circ \times \delta$ , wherein the frequency shift  $\delta$  is obtained by dividing the frequency difference by a frequency of the predetermined sampling clock and is represented in form of  $RN / 2^n$  ( $RN$  is an rational number).

The converter preferably performs a conversion operation according to the following steps:

Step 1)  $k = -1$  and  $\Phi_k = \Phi$ ;  
 Step 2)  $D_k = \text{sign bit of } \Phi_k$ ;  
 Step 3) if  $k = m - 2$ , then exit, else go to step 4);  
 Step 4)  $\Phi_{k+1} = \Phi_k - \theta_k$  when  $D_k = 0$ , and  
 $\Phi_{k+1} = \Phi_k + \theta_k$  when  $D_k = 1$ ,  
 where  $\theta_k = \arctan(2^{-k})$ ;  
 Step 5)  $k = k + 1$ ; and  
 Step 6) go to step 3).

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The signal vector rotator preferably includes a plurality of partial rotators  $R_k$  which are connected in series in descending order of a rotation angle, wherein the partial rotators  $R_k$  receive the control bits  $D_k$ , respectively, and each of the partial

5 rotators  $R_k$  rotates an output of a previous stage  $R_{k-1}$  by a predetermined angle depending on a corresponding control bit received from the converter.

In the plurality of partial rotators, a first partial rotator  $R_1$  rotates an input signal vector  $(I_{in}, Q_{in})$  by an angle

10  $\theta_1$  to produce a first output signal vector  $(I_{out,1}, Q_{out,1})$  as follows:  $I_{out,1} = D_{-1} \times Q_{in}$  and  $Q_{out,1} = -D_{-1} \times I_{in}$ .

Further, each of partial rotators  $R_k$  ( $0 \leq k \leq m-2$ ) rotates an input signal vector  $(I_{in,k}, Q_{in,k})$  by an angle  $\theta_k$  to produce an output signal vector  $(I_{out,k}, Q_{out,k})$  as follows:

15 
$$I_{out,k} = I_{in,k} + 2^{-k} \times D_k \times Q_{in,k} \text{ ; and}$$

$$Q_{out,k} = -2^{-k} \times D_k \times I_{in,k} + Q_{in,k} \text{ ,}$$

where  $D_k$  uses numerical value representation such that a numerical value "1" is represented by a logical value "1" and a numerical value "-1" is represented by a logical value "0".

20 The signal vector rotator rotates an input signal vector  $(I_{in}, Q_{in})$  having an absolute value  $Z_{in}$  by an angle  $\Theta$  while the absolute value  $Z_{in}$  becomes  $Z_{out}$ , where  $\Theta$  and  $Z_{out}$  are represented as follows:

$$\Theta = D_{-1} \times 90^\circ + \sum_{k=0}^{m-2} D_k \cdot \arctan(2^{-k}) \quad \text{and}$$

$$Z_{out} = \frac{Z_{in}}{\prod_{k=0}^{m-2} \cos \theta_k}$$

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Since a signal vector determined by the input I and Q components is rotated around the origin of the I-Q plane to be frequency-shifted to the center carrier band, the respective signal vectors of the frequency bands are obtained in the center  
5 carrier band.

Further, in multi carrier communications, especially in multi-carrier CDMA communications, the present invention can provide a frequency shifting circuit without the need of ROM and multiplier, which is simplified, reduced in power  
10 consumption, and suitable for a small-sized portable terminal. Since the frequency shifting circuit rotates a signal vector on the I-Q plane by means of digital computation, it is possible to demodulate received signals in the upper and lower bands into signals in the center band with extremely high precision.

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#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a circuit of a demodulation circuit employing a frequency shifting circuit according to an embodiment of the present invention;

FIG. 2 is a block diagram showing a phase accumulator used  
20 in the frequency shifting circuit of FIG. 1;

FIG. 3A is a block diagram showing a counter used in the phase accumulator of FIG. 2;

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FIG. 3B is a timing chart showing a relationship between a sampling-rate clock and an output of the counter:

FIG. 4 is a block diagram showing a frequency shift control signal generator used in the frequency shifting circuit of FIG.

5 1;

FIG. 5 is a block diagram showing a de-rotator used in the frequency shifting circuit of FIG. 1;

FIG. 6 is a block diagram showing a rotator used in the frequency shifting circuit of FIG. 1;

10 FIG. 7 is a block diagram showing a partial rotation circuit used in the rotator and the de-rotator;

FIG. 8 is a block diagram showing an initial rotation circuit used in the rotator and the de-rotator;

15 FIG. 9 is a table showing correspondence between a partial rotation angle and its cosine in each stage of the partial rotation circuits in each of the rotator and the de-rotator; and

FIG. 10 is a schematic diagram showing an example of a power spectrum of a multi-carrier signal.

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## DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereafter, a preferred embodiment of the present invention will be described by referring to the drawings.

A frequency shifting demodulation circuit according to the present invention includes a well-known quadrature frequency converter (not shown) that reproduces in phase (I) components and Quadrature (Q) components from received signals according to the quadrature modulation scheme.

Here, it is assumed, as shown in Fig. 10, that the I and Q components are reproduced from received signals on the center carrier and the two sub-carriers. Frequencies of the sub-carriers are shifted from the center carrier by the same amounts in the lower-frequency and higher-frequency directions, respectively. In this example, the frequency offset of each sub-carrier is 1.25 MHz and the chip rate is 1.2288 Mcps. As described before, since the number of carriers is 3, a maximum data rate of 43.2 kbps can be obtained.

As shown in FIG. 1, the frequency shifting demodulation circuit further includes an analog-to-digital (A/D) converter 101 which causes the input I and Q components to be converted into digital form according to a sampling rate clock having a sampling rate which is eight times the chip rate. The A/D converter 101 outputs digital I and Q components to each of a de-rotator (or a negative frequency shifter) 102, a non-

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rotator(or a non-shifter) 103, and a rotator(or a positive frequency shifter) 104. The de-rotator 102, the non-rotator 103, and the rotator 104 are connected to finite impulse response (FIR) filters 105, 106 and 107, respectively. The FIR filters 105, 106 and 107 have the same band-pass filtering characteristic for the center carrier Carrier-0 and output signals  $I_1$  and  $Q_1$  for higher sub-carrier Carrier+1, signals  $I_2$  and  $Q_2$  for center carrier Carrier-0, and signals  $I_3$  and  $Q_3$  for lower sub-carrier Carrier-1 to corresponding despreaders (not shown), respectively. As described later, a phase accumulator 108 generates phase data  $\Phi$  from a predetermined sampling rate clock and a frequency shift control signal generator 109 converts the phase data  $\Phi$  to frequency shift control data D and outputs it to each of the de-rotator 102 and the rotator 104.

The de-rotator 102 decreases the frequency of I and Q components from the frequency of the sub-carrier Carrier+1 to the center carrier frequency band by rotating a signal point determined by the I and Q components for the sub-carrier Carrier+1 around the origin of an I-Q plane. Here, the amount of frequency shift is -1.25MHz. The non-rotator 103 does not shift the frequency of the center carrier but performs gain and timing compensation. The rotator 102 increases the frequency of I and Q components from the frequency of the sub-carrier Carrier-1 to the center carrier frequency band by rotating a signal point determined by the I and Q components for the sub-carrier Carrier-1. Here, the amount of frequency shift is +1.25MHz.

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Phase accumulator

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one chip is sampled by eight-times oversampling compared with the chip rate. Further, it is assumed that the frequency shift of each sub-carrier from the center carrier is 1.25 MHz. At this time, a frequency shift  $\delta$  per sample is  $1.25 \text{ MHz} / (1.2288$

5 Mchips/sec  $\times$  8 samples/chip), which is approximately 0.127/sample. Therefore, a product  $\Delta$  of  $\delta$  and 360 degrees is approximately 45.7 degrees. By taking  $\Delta$  as a unit angle, phases in the range of 360 degrees ranging from -180 degrees to +180 degrees are represented by, for example, 13-bit binary numbers.

10 In other words, 360 degrees are divided into  $2^{12}$  (= 4096) parts. Thus,  $2^{12}$  (= 4096) angle indication points are provided at equal intervals between -180 degrees and 0 degree, and  $2^{12}$  (= 4096) angle indication points are provided at equal intervals between 0 degree and +180 degrees. Representing  $(\Delta/360)$  approximately  
15 by using " $2^{13}$ ", we get  $(1041 + 2/3) / 2^{13}$ . Converting the decimal number "1041" to a 13-bit binary number Z, we get "0 0100 0001 0001".

As shown in FIG. 2, the full adder 203 is supplied with an output of the 13-bit register 204 as its input A, and is further  
20 supplied with the above-described binary number Z, i.e., the decimal number 1041 (hereafter, simply referred to as "1041") as its input B. The full adder 203 adds the A input and the B input which is 1041. Thus, " $A + 1041$ " is calculated. Further, to add the fraction  $2/3$  to the result " $A + 1041$ ", that is, to  
25 calculate " $A + (1041 + 2/3)$ ", the carry signal W output from the counter 202 is input to a carry terminal C of the full adder 203.

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Eventually, the result of " $A + (1041 + 2/3)$ " is output from the 13-bit register 204 as phase data  $\Phi$ . The 13-bit register 204 holds the output of the full adder 203 at timing (e.g. leading edge) of the sampling-rate clock. In this way, the phase

5 accumulator 108 produces phase data  $\Phi$  as a binary number equal to the product of the unit angle  $\Delta$  and a natural number in synchronism with the sampling-rate clock.

Referring to FIG. 3A, the counter 202 is composed of two D-type flip-flop circuits 301 and 302 and an NOR gate 303. The

10 output Q of the flip-flop circuit 301 is connected to the input D of the flip-flop circuit 302 and the one input of the NOR gate 303. The other input of the NOR gate 303 is connected to the output Q of the flip-flop circuit 302. The output of the NOR gate 303 is connected to the input D of the flip-flop circuit

15 301. The sampling-rate clock is supplied to both the clock terminals of the flip-flop circuits 301 and 302. The inverted output QB of the flip-flop circuit 302 is output as the carry signal W to the carry input C of the full adder 203. In this example, the counter 202 divides the frequency of the

20 sampling-rate clock by  $N = 3$ .

As shown in Fig. 3B, the carry signal W, that is, the output of the counter 202 is "1" during two clock periods of the sampling-rate clock, and "0" during one clock period of the sampling-rate clock. Therefore, when the full adder 203 inputs

25 the carry signal W at its carry input C from the count 202, 2 is added to  $(A + B)$  every three clock periods. As a result,  $2/3$  is added to the output of the full adder 203 per clock period.

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Freq. shift control signal generator

Referring to FIG. 4, the frequency shift control signal generator 109 receives the phase data  $\Phi$  from the phase accumulator 108, generates thirteen partial phases ( $\Phi_1, \Phi_0, \Phi_{-1}, \dots, \Phi_{-10}, \Phi_{-11}$ ) and thirteen control signals D ( $D_1, D_0, D_{-1}, \dots, D_{-10}, D_{-11}$ ).

Hereafter, an algorithm for generating the control signals D on the basis of the phase data  $\Phi$  will be described. In Fig. 4, functional blocks for implementing the algorithm are shown.

10 The algorithm is constructed by the following steps:

Step 1)  $k = -1$  and  $\Phi_k = \Phi$ ;

Step 2)  $D_k = \text{sign bit of } \Phi_k$ ;

Step 3) if  $k = 11$ , then exit, else go to step 4);

Step 4)  $\Phi_{k+1} = \Phi_k - \theta_k$  when  $D_k = 0$ , and

15  $\Phi_{k+1} = \Phi_k + \theta_k$  when  $D_k = 1$ ;

Step 5)  $k = k + 1$ ; and

Step 6) go to step 3).

More specifically,  $k$  is set to  $-1$  and the phase  $\Phi$  is set as  $\Phi_{-1}$ . If  $\Phi_{-1}$  has a positive value, then the most significant bit (MSB)  $D_{-1}$  of the control signal D is set to a logical value "1" and  $\Phi_0$  is set to  $\Phi_{-1} + 90$ . If  $\Phi_{-1}$  has a negative value, then  $D_{-1}$  is set to a logical value "0" and  $\Phi_0$  is set to  $\Phi_{-1} - 90$ .

Subsequently, it is determined whether the numerical value  $\Phi_0$  obtained earlier is positive or negative. If  $\Phi_0$  has a positive value, then the logical value of  $D_0$  is set to 1 and  $\Phi$

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is set to  $\Phi_0 + \theta_0$ . If  $\Phi_0$  has a negative value, then  $D_0$  is set to a logical value "0" and  $\Phi_1$  is set  $\Phi_1 = \Phi_0 - \theta_0$ , where  $\theta_0 = \arctan(2^0)$ . Generally,  $\theta_k = \arctan(2^{-k})$ .

In succession, it is determined whether  $\Phi_1$  is positive or negative. If  $\Phi_1$  has a positive value, then the logical value of  $D_1$  is set to 1 and  $\Phi_2$  is set to  $\Phi_1 + \theta_1$ . If  $\Phi_1$  has a negative value, then  $D_1$  is set to a logical value "0" and  $\Phi_2$  is set to  $\Phi_1 - \theta_1$ .

Here,  $\theta_k$  to be added to or subtracted from  $\Phi_k$  is supplied by twelve data selectors as indicated by reference numerals 401 to 404 depending on the sign bit of  $\Phi_k$ , that is,  $\Phi_k$  is positive or negative. If  $\Phi_k$  is positive, then  $-\theta_k$  is supplied to a corresponding adder. When  $\Phi_k$  is negative, then  $+\theta_k$  is supplied to the corresponding adder. Generally, if  $D_k$  has a logical value "0", then  $\Phi_{k+1} = \Phi_k - \theta_k$ . If  $D_k$  has a logical value "1", then  $\Phi_{k+1} = \Phi_k + \theta_k$ .

By generating  $\Phi_k$  in this manner, the numerical value of  $\Phi_k$  can be brought closer to 0 successively as close as possible. There is improved the precision of approximation of the rotation angle  $\odot$  by which a signal vector in the I-Q plane is rotated. Generally, if the value of  $k$  becomes larger, then  $\arctan(2^{-k})$  is assumed to be approximately  $2 \times \arctan(2^{-k-1})$ . Therefore, this method is more effective.

#### Rotator and De-rotator

Referring to FIG. 5, the rotator 104 is designed to rotate



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control signals  $D_{-1}$ ,  $D_0$ ,  $D_1$ , ...,  $D_{10}$ ,  $D_{11}$  are provided to the partial rotation circuits  $R_{-1}$ ,  $R_0$ ,  $R_1$ , ...,  $R_{10}$ ,  $R_{11}$ .

10 D<sub>0</sub>, D<sub>1</sub>, ... The de-rotator 102 is composed of the same partial rotation circuits R<sub>-1</sub>, R<sub>-2</sub>, R<sub>-3</sub>, ..., R<sub>-10</sub>, R<sub>-11</sub> as those used in the rotator 104 and inverters INV<sub>-1</sub>, INV<sub>-2</sub>, INV<sub>-3</sub>, ..., INV<sub>-10</sub>, INV<sub>-11</sub>. The respective control signals D<sub>-1</sub>, D<sub>-2</sub>, D<sub>-3</sub>, ..., D<sub>-10</sub>, D<sub>-11</sub> are connected to the partial rotation circuits R<sub>-1</sub>, R<sub>-2</sub>, R<sub>-3</sub>, ..., R<sub>-10</sub>, R<sub>-11</sub> through the inverters INV<sub>-1</sub>, INV<sub>-2</sub>, INV<sub>-3</sub>, ..., INV<sub>-10</sub>, INV<sub>-11</sub>.

the initial stage receives the  $I_{in}$  and  $Q_{in}$  component signals from the A/D converter 101, and outputs  $Q_{out,-1}$  and  $I_{out,-1}$  component signals to the partial rotation circuit  $R_0$  at the next stage.

25 supplies its output to the multiplier 802.

the partial rotation circuit  $R_i$  are represented by the following

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equation (1):

$$\begin{aligned} I_{out,-1} &= D_{-1} \times Q_{in} \quad \text{and} \\ Q_{out,-1} &= -D_{-1} \times I_{in} \end{aligned} \quad (1),$$

where  $D_{-1}$  uses numerical value representation such that a  
 5 numerical value "1" is represented by the logical value "1" and  
 a numerical value "-1" is represented by the logical value "0".

The partial rotation circuit  $R_{-1}$  is a circuit for rotating  
 the signal vector  $(I, Q)$  by an angle  $\theta_{-1}$ . According to the  
 equation (1),  $\theta_{-1}$  is plus 90 degrees when the numerical value  
 10 of the control signal  $D_{-1}$  is "-1" and  $\theta_{-1}$  is minus 90 degrees when  
 the numerical value of the control signal  $D_{-1}$  is "1". In this  
 way, the partial rotation circuit  $R_{-1}$  rotates the signal vector  
 without changing the absolute value of the signal vector.

Referring to FIG. 8, a partial rotation circuits  $R_k$  which  
 15 is any of the partial rotation circuits  $R_0$  to  $R_{11}$  is a circuit  
 which receives  $Q_{in,k}$  and  $I_{in,k}$  from the previous stage and outputs  
 $Q_{out,k}$  and  $I_{out,k}$ . The partial rotation circuit includes two  
 constant multipliers 701 and 704, two multipliers 702 and 705,  
 and two adders 703 and 706. The signal  $I_{in,k}$  is input to the adder  
 20 703 and the constant multiplier 701. The output of the constant  
 multiplier 701 is multiplied by a corresponding control signal  
 $D_k$  at the multiplier 702. The output of the multiplier 702 is  
 inverted in sign and input to the adder 706. The signal  $Q_{in,k}$  is  
 input to the adder 706 and the constant multiplier 704. The  
 25 output of the constant multiplier 704 is multiplied by a  
 corresponding control signal  $D_k$  at the multiplier 705. The  
 output of the multiplier 705 is input to the adder 703. In other

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$$I_{out,k} = I_{in,k} + 2^{-k} \times D_k \times Q_{in,k} \quad \text{and}$$

where  $D_k$  uses numerical value representation such that a numerical value "1" is represented by the logical value "1" and a numerical value "-1" is represented by the logical value "0".

20           Heretofore, the partial rotation circuits have been described. The rotator 104 is a circuit formed by cascade-connecting thirteen partial rotation circuits ( $R_{11}, R_{12}, R_{13}, \dots, R_{1n}, R_{1n+1}$ ). When a signal vector ( $I, Q$ ) having an absolute value  $Z_{in}$  is input to the rotator 104, the signal vector is rotated

25   by an angle  $\Theta$  and its absolute value becomes  $Z_{out}$  to output it from the rotator 104. The angle  $\Theta$  and  $Z_{out}$  are represented by the following equations (3) and (4).

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$$\Theta = D_{-1} \times 90^\circ + \sum_{k=0}^{11} D_k \cdot \arctan(2^{-k}) \quad (3)$$

$$Z_{out} = \frac{Z_{in}}{\prod_{k=0}^{11} \cos \theta_k} \quad (4)$$

FIG. 9 is a table showing correspondence relations among  
 5  $K$ ,  $2^k$ ,  $\theta_k$ ,  $\cos \theta_k$ , and  $15 \times 2^k$ . According to the table, the  
 denominator of the right side of the equation (4) is a constant  
 0.6072529591.

As described above, in multi-carrier communications, in  
 particular, multi-carrier CDMA communications, the present  
 10 invention heretofore described provides a frequency shifting  
 circuit which is simplified, reduced in power consumption, and  
 suitable for a small-sized portable terminal. Since the  
 frequency shifting circuit rotates a signal vector on the I Q  
 plane by means of digital computation, it is possible to  
 15 demodulate received signals in the upper and lower bands into  
 signals in the center band with extremely high precision.

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1. A digital circuit for shifting a frequency band of a signal vector to a predetermined frequency band, wherein the signal vector is determined by a pair of I (in-phase) and Q (quadrature) components on I-Q plane, comprising:

a signal vector rotator for rotating the signal vector on the I-Q plane by an angle determined depending on the control data to produce an output signal vector in the predetermined frequency band.

an analog-to-digital converter for converting a  
15 received analog signal vector to the signal vector according  
to a predetermined sampling clock,

a phase data generator for generating phase data from the frequency difference in synchronization with the predetermined sampling clock; and

a converter for converting the phase data to the control data consisting of a plurality of control bits.

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3. The digital circuit according to claim 2, wherein the signal vector rotator comprises:

a plurality of partial rotators which are connected in series in descending order of a rotation angle, wherein each of the partial rotators receives a different bit of the control bits of the control data and rotates an output of a previous stage by a predetermined angle depending on a corresponding control bit received from the converter.

4. The digital circuit according to claim 2, wherein the phase data generator generates the phase data by computing an integral multiple of a unit angle which is obtained from a frequency shift per period of the predetermined sampling clock.

5. A digital circuit for shifting a plurality of frequency bands of input signal vectors to a predetermined center frequency band to produce an output signal vector for each frequency band, wherein each of the input signal vectors is determined by a pair of I (in-phase) and Q (quadrature) components on I-Q plane, comprising:

an analog-to-digital converter for converting analog signal vectors to the input signal vectors according to a predetermined sampling clock;

a control data generator for generating control data from a frequency difference between each of the plurality of frequency bands and the predetermined center frequency band;

a signal vector rotator corresponding to each of the

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5 and

a phase data generator for generating phase data  $\Phi$  from the frequency difference in synchronization with the predetermined sampling clock; and

7. The digital circuit according to claim 6, wherein the phase data generator generates the phase data  $\Phi$  by computing an integral multiple of a unit angle  $\Delta$  which is obtained from a frequency shift  $\delta$  per period of the predetermined sampling clock, wherein the unit angle  $\Delta$  is represented by  $360^\circ \times \delta$ , wherein the frequency shift  $\delta$  is obtained by dividing the frequency difference by a frequency of the predetermined sampling clock and is represented in form of  $RN / 2^n$  ( $RN$  is an

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rational number).

8. The digital circuit according to claim 7, wherein the converter performs a conversion operation according to the following steps:

- 5        Step 1)  $k = -1$  and  $\Phi_k = \Phi$ ;  
       Step 2)  $D_k$  - sign bit of  $\Phi_k$ ;  
       Step 3) if  $k = m - 2$ , then exit, else go to step 4);  
       Step 4)  $\Phi_{k+1} = \Phi_k - \theta_k$  when  $D_k = 0$ , and  
                $\Phi_{k+1} = \Phi_k + \theta_k$  when  $D_k = 1$ , where  $\theta_k = \arctan(2^{-k})$ ;  
 10        Step 5)  $k = k + 1$ ; and  
       Step 6) go to step 3).

9. The digital circuit according to claim 8, wherein the signal vector rotator comprises:

- a plurality of partial rotators  $R_k$  which are  
 15        connected in series in descending order of a rotation angle,  
       wherein the partial rotators  $R_k$  receive the control bits  $D_k$ ,  
       respectively, and each of the partial rotators  $R_k$  rotates an  
       output of a previous stage  $R_{k+1}$  by a predetermined angle depending  
       on a corresponding control bit received from the converter.

- 20        10. The digital circuit according to claim 9, wherein  
       a first partial rotator  $R_{-1}$  rotates an input signal vector  
        $(I_{in}, Q_{in})$  by an angle  $\theta_{-1}$  to produce a first output signal vector  
        $(I_{out,-1}, Q_{out,-1})$  as follows:

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$$I_{out,-1} = D_{-1} \times Q_{in} ; \text{and}$$

$$Q_{out,-1} = -D_{-1} \times I_{in} ,$$

each of partial rotators  $R_k$  ( $0 \leq k \leq m-2$ ) rotates an input  
 signal vector  $(I_{in,k} , Q_{in,k})$  by an angle  $\theta_k$  to produce an output  
 5 signal vector  $(I_{out,k} , Q_{out,k})$  as follows:

$$I_{out,k} = I_{in,k} + 2^{-k} \times D_k \times Q_{in,k} \quad \text{and}$$

$$Q_{out,k} = -2^{-k} \times D_k \times I_{in,k} + Q_{in,k} ,$$

where  $D_k$  uses numerical value representation such that a  
 numerical value "1" is represented by a logical value "1" and  
 10 a numerical value "-1" is represented by a logical value "0".

11. The digital circuit according to claim 9, wherein  
 the signal vector rotator rotates an input signal vector  $(I_{in},$   
 $Q_{in})$  having an absolute value  $Z_{in}$  by an angle  $\Theta$  while the absolute  
 value  $Z_{in}$  becomes  $Z_{out}$ , where  $\Theta$  and  $Z_{out}$  are represented as follows:

$$\Theta = D_{-1} \times 90^\circ + \sum_{k=0}^{m-2} D_k \cdot \arctan(2^{-k}) \quad \text{and}$$

$$Z_{out} = \frac{Z_{in}}{\prod_{k=0}^{m-2} \cos \theta_k} .$$

12. A digital demodulator for use in a multi-carrier CDMA  
 (code division multiple access) communication system, for  
 shifting two carrier bands of input signal vectors to a center  
 20 carrier band to produce an output signal vector for each carrier  
 band, wherein each of the input signal vectors is determined

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a quadrature frequency converter for converting a received high frequency signal to analog signal vectors having I component and Q component;

a control data generator for generating control data  
10 from a frequency difference between each of the plurality of  
frequency bands and the predetermined center frequency band;

a band-pass filter corresponding to the signal  
vector rotator, for receiving an output of the signal vector  
20 rotator and passing an output signal vector of the predetermined  
center frequency band.

generating control data from a frequency difference

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between the frequency band and the predetermined frequency band;  
and

rotating the signal vector on the I-Q plane by an  
angle determined depending on the control data to produce an  
5 output signal vector in the predetermined frequency band.

14. A method for shifting a plurality of frequency bands  
of input signal vectors to a predetermined center frequency band  
to produce an output signal vector for each frequency band,  
wherein each of the input signal vectors is determined by a pair  
10 of I (in-phase) and Q (quadrature) components on I-Q plane,  
comprising:

converting analog signal vectors to the input signal  
vectors according to a predetermined sampling clock;

generating control data from a frequency difference  
15 between each of the plurality of frequency bands and the  
predetermined center frequency band;

rotating the input signal vectors on the I-Q plane  
by an angle determined depending on corresponding control data  
to shift the frequency bands of the input signal vectors to the  
20 predetermined center frequency band; and

filtering frequency bands other than the  
predetermined center frequency band from an output of the signal  
vector rotator to pass an output signal vector of the  
predetermined center frequency band.

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## ABSTRACT

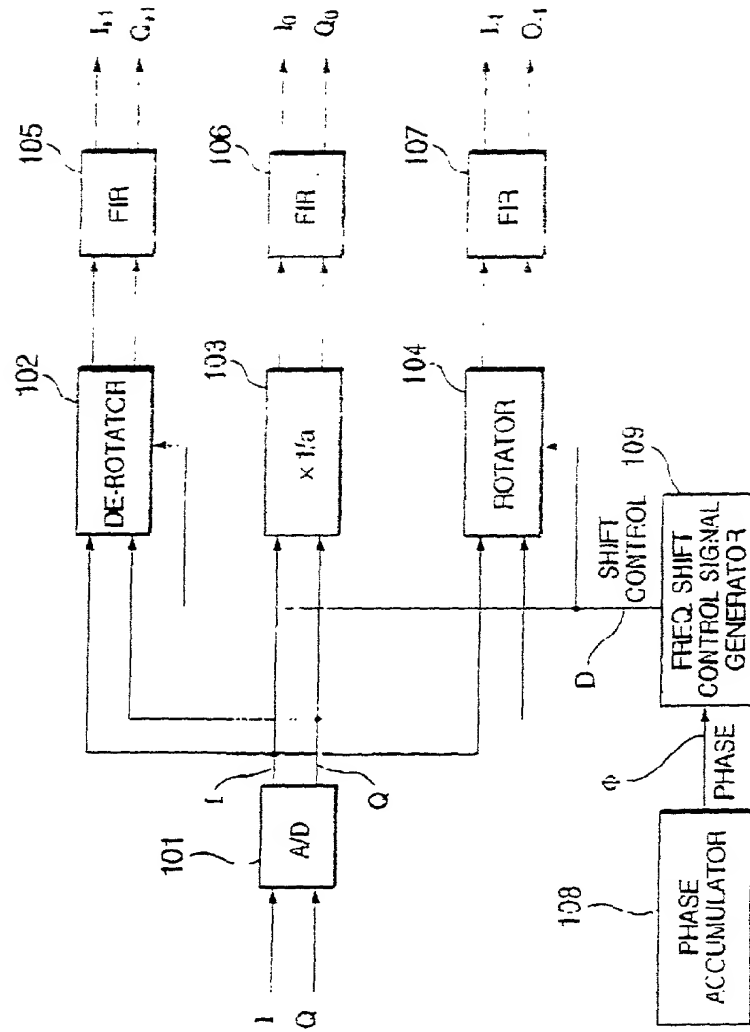
A frequency shifting circuit suitable for a digital demodulator in a multi-carrier communications system is disclosed. After converting analog signal vectors to the input signal vectors according to a predetermined sampling clock, control data is generated from a frequency difference between sub carrier bands and center carrier band. A signal vector rotator is provided corresponding to each of the sub-carrier bands and rotates the input signal vectors on the I Q plane by an angle determined depending on corresponding control data to shift the sub-carrier bands of the input signal vectors to the center carrier band. A band-pass filter passes an output signal vector of the center carrier band.

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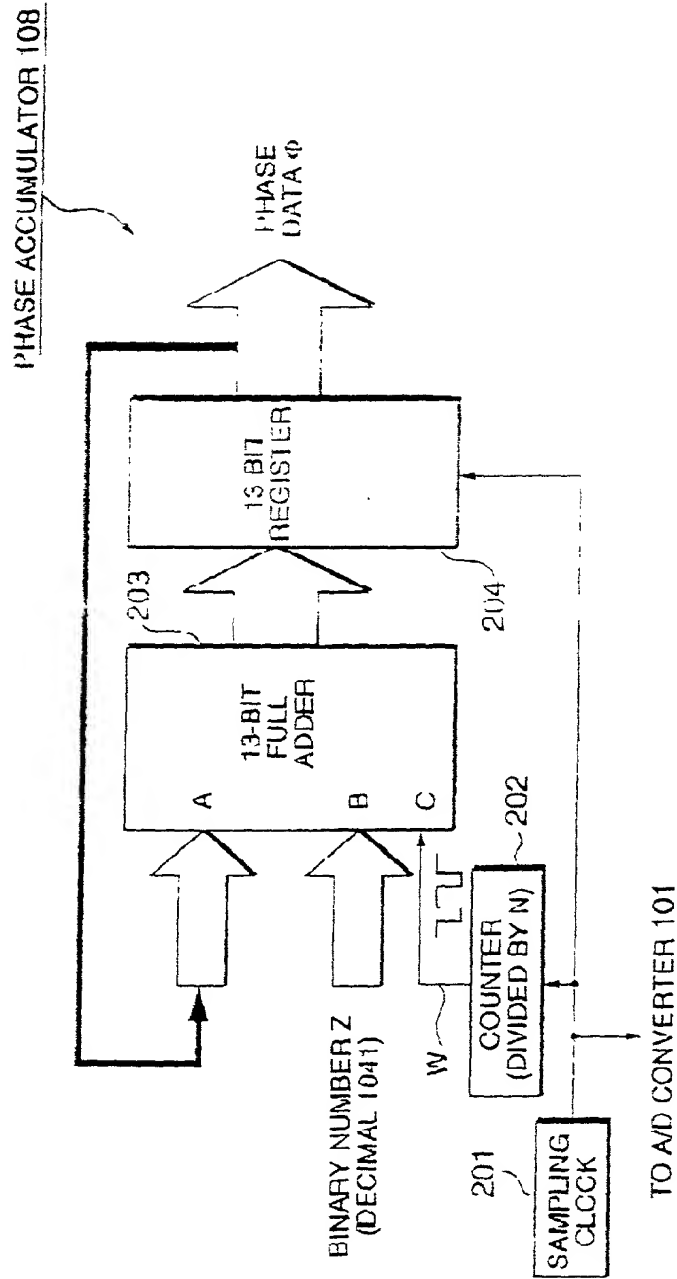
FIG. 1



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FIG. 2



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FIG. 3A

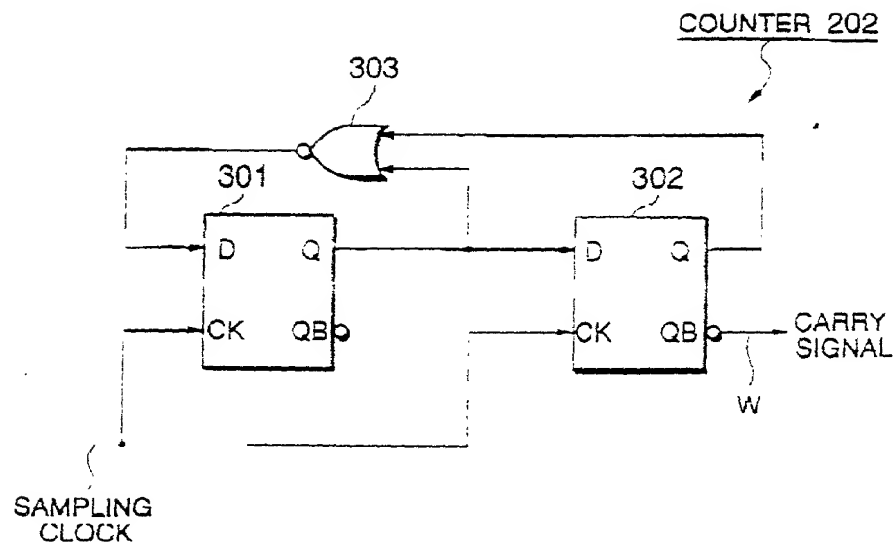
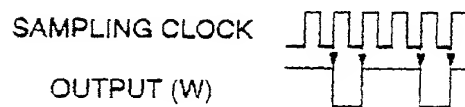
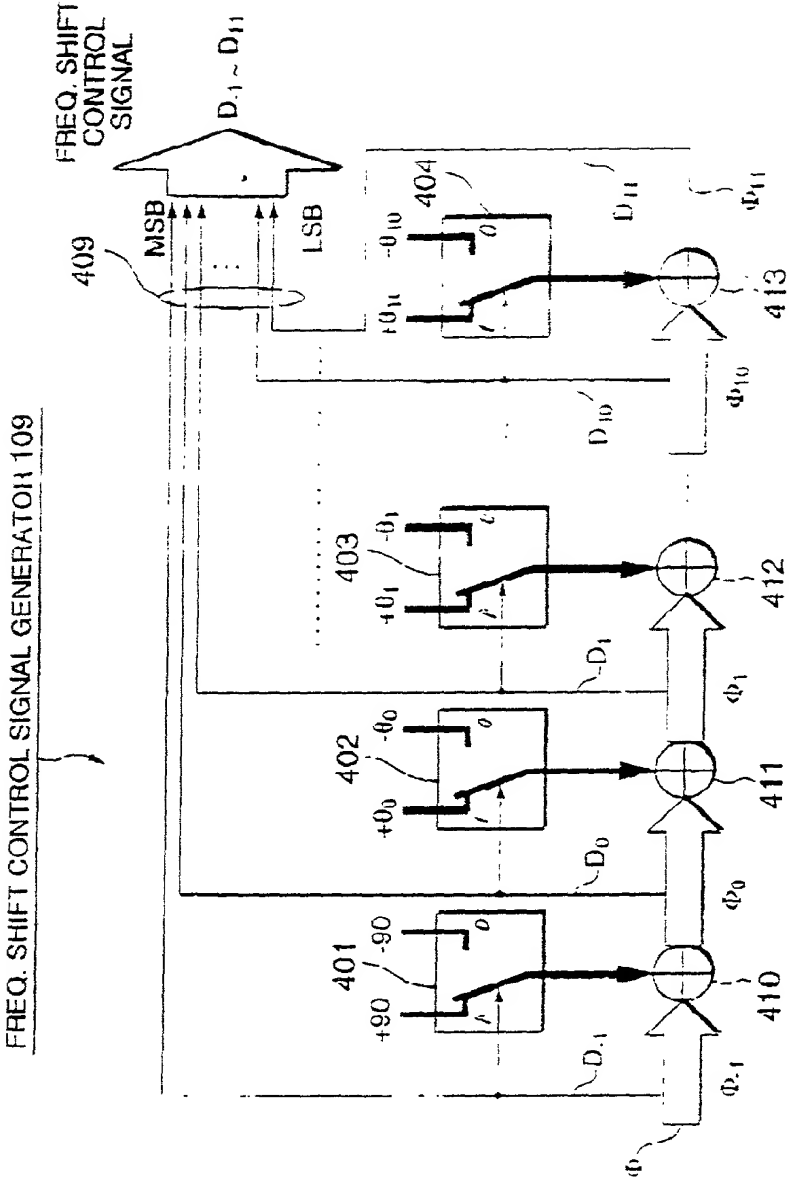


FIG. 3B



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FIG. 4





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FIG. 5

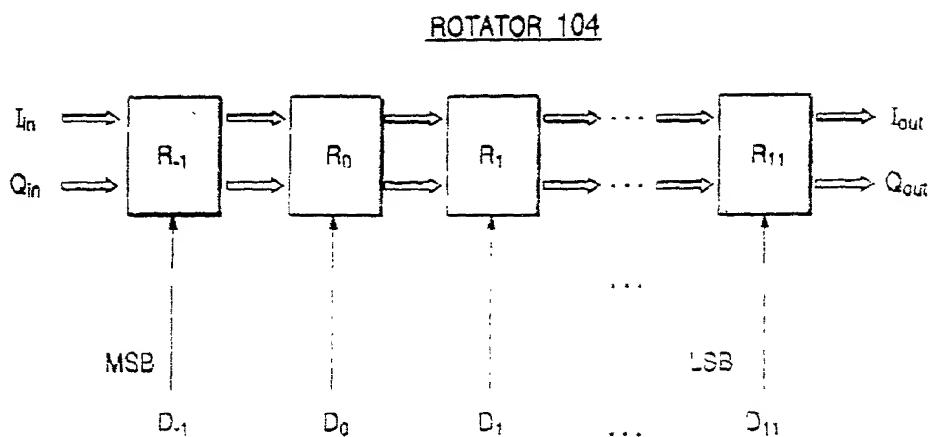
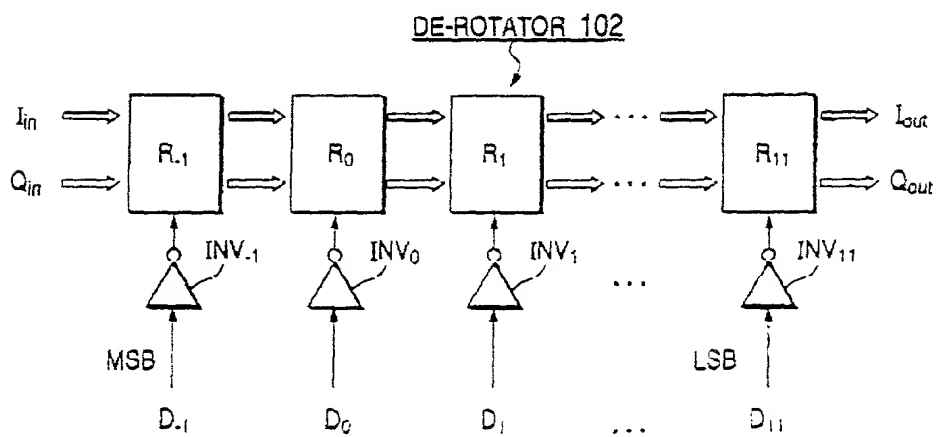


FIG. 6



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FIG. 7

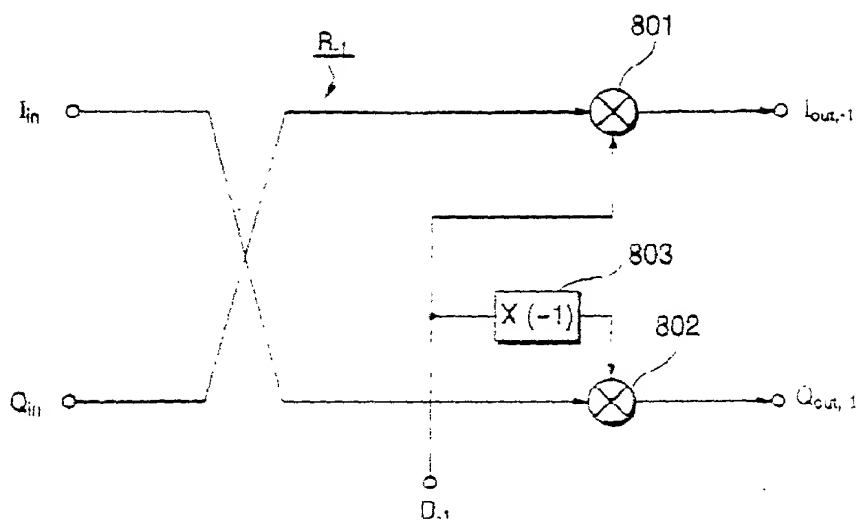
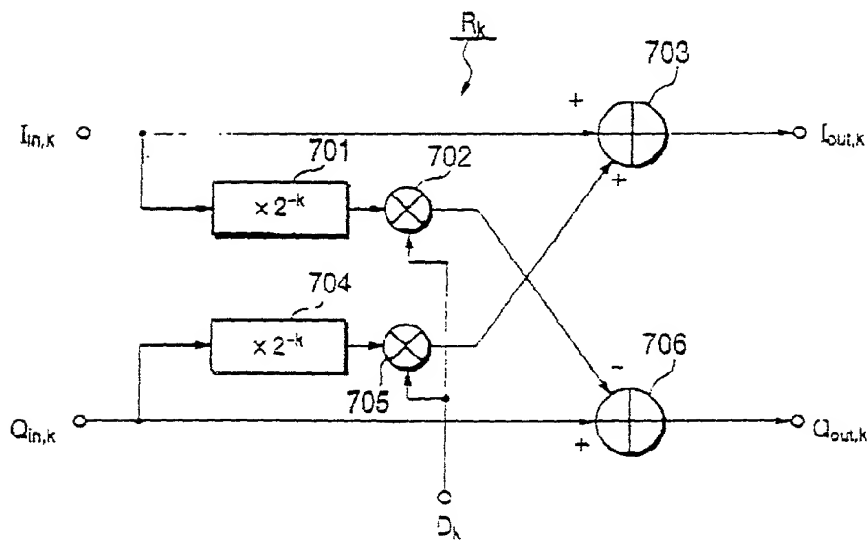


FIG. 8



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FIG. 9

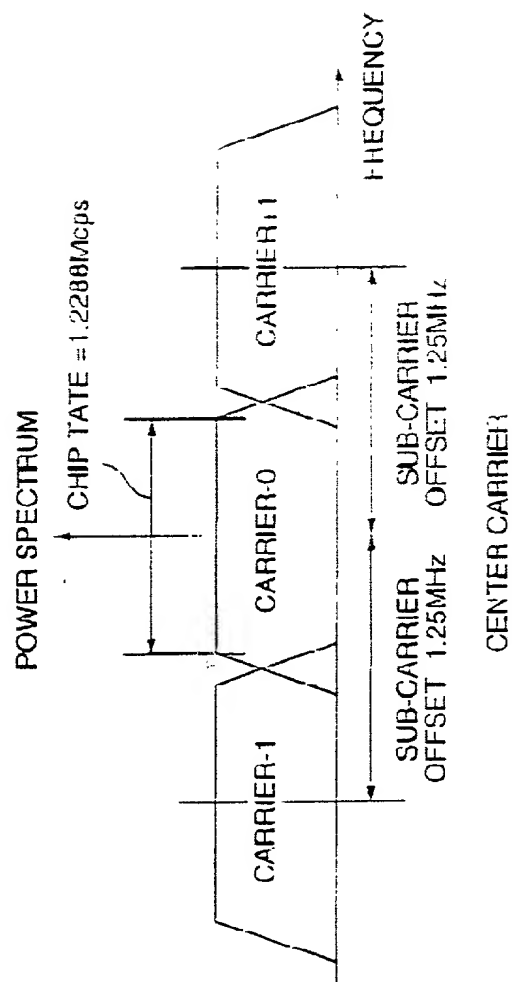
k	$2^{-k}$	$\theta_k = \arctan(2^{-k})$	$\cos \theta_k$	$45 \times 2^{-k}$
0	1.000000000	45.000000000	0.7071067812	45.0000000000
1	0.500000000	26.5650511771	0.8944271910	22.5000000000
2	0.250000000	14.0362434679	0.9701425001	11.2500000000
3	0.125000000	7.1250163489	0.9922778767	5.6250000000
4	0.062500000	3.5763343750	0.9980525785	2.8125000000
5	0.031250000	1.7899106082	0.9995120761	1.4062500000
6	0.015625000	0.8951737102	0.9998773520	0.7031250000
7	0.007812500	0.4476141709	0.9999604838	0.3515625000
8	0.003906250	0.2236105004	0.9999923707	0.1757812500
9	0.001953125	0.1119056771	0.9999980927	0.0878906250
10	0.0009765625	0.0559528919	0.9999995232	0.0439453125
11	0.0004882813	0.0279764526	0.9999998808	0.0219726563
12	0.0002441406	0.0139862271	0.9999999702	0.0109863281
13	0.0001220703	0.0069941137	0.9999999925	0.0054931641
14	0.0000610352	0.0034970569	0.9999999981	0.0027465820
15	0.0000305176	0.0017465284	0.9999999995	0.0013732910

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FIG. 10



UNITED STATES OF AMERICA		OFGS FILE NO.	
COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION		P/2291-85	
<p>As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:</p> <p style="text-align: center;"><b>FREQUENCY SHIFTING CIRCUIT AND METHOD</b></p>			
<p>the specification of which is attached hereto, unless the following box is checked:</p> <p><input type="checkbox"/> was filed on _____ as United States patent Application Number or PCT International patent Number _____ and was amended on _____ (if any).</p> <p>I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.</p> <p>I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.</p> <p>I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:</p>			
Prior Foreign or Provisional Application(s)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Japan	108333/1999	15.04.1999	YES <input checked="" type="checkbox"/> NO <input type="checkbox"/>
			YES <input type="checkbox"/> NO <input type="checkbox"/>
			YES <input type="checkbox"/> NO <input type="checkbox"/>
<p>I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.</p>			
UNITED STATES APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)	
<p>I hereby appoint OSTROLENK, FABER, GERB &amp; SOFFEN, and the members of the firm, Marvin C. Soffen - Reg. No. 17,542; Samuel H. Weiner - Reg. No. 18,510; Jerome M. Borliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A. Moilman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,400; Steven I. Weisburd - Reg. No. 27,409; Max Moskowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063; James A. Finder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944 and Louis C. Dujnach - Reg. No. 30,625, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent &amp; Trademark Office connected therewith and to receive all correspondence.</p>			
SEND CORRESPONDENCE TO:		DIRECT TELEPHONE CALLS TO:	
OSTROLENK, FABER, GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NEW YORK 10036-8403		(212) 382-0700	
<p>I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.</p>			
FULL NAME OF SOLE OR FIRST INVENTOR		INVENTOR'S SIGNATURE	DATE
MASAKI ICHIHARA		Masaki Ichihara	April 7, 2000
RESIDENCE		COUNTRY OF CITIZENSHIP	
Tokyo, Japan		Japan	
POST OFFICE ADDRESS			
c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo, Japan			
FULL NAME OF SECOND JOINT INVENTOR (if any)		INVENTOR'S SIGNATURE	DATE
RESIDENCE		COUNTRY OF CITIZENSHIP	
POST OFFICE ADDRESS			
FULL NAME OF THIRD JOINT INVENTOR (if any)		INVENTOR'S SIGNATURE	DATE
RESIDENCE		COUNTRY OF CITIZENSHIP	
POST OFFICE ADDRESS			

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